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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	6

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/838,610	MILLER ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally **limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length** since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

1. The abstract of the disclosure is objected to because the Abstract exceeds 150 words. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 3, 4, 9 and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 3 and 16 substantially recite, "Berlekamp-Massey module carries out repeated dot product calculations between vectors with up to T+1 components". It is not clear whether the "T+1 components" refer

to the "Berlekamp-Massey module", the "repeated dot product calculations" or the "vectors".

Claim 4 recites the limitation "each dot product" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 4 recites "to carry out each dot product calculation in a single step", which is ambiguous since the term "step" is a relative and can include many sub-steps.

Claim 9 recites the limitation "dual-mode operation" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-6, 8, 10, 11, 13-17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okita; Shigeru (US 6378104 B1) in view of Cameron; Kelly (US 6317858 B1).

35 U.S.C. 103(a) rejection of claims 1 and 14.

Okita teaches a Reed-Solomon BCH error correction decoder for decoding a predetermined number of Reed-Solomon and BCH codes (col. 5, 26-37 and Figure 1 in Okita is a Reed-Solomon error correction decoder for decoding a predetermined number of Reed-Solomon codes; Note: Reed Solomon codes are a subclass of generalized BCH codes, hence Reed Solomon codes are generalized BCH codes), said decoder comprising: a translator circuit for receiving one of the predetermined number of Reed-Solomon and BCH codes that each have predetermined external Galois-field representations and for translating the external Galois-field representation of the received code into an internal Galois-field representation (Figure 1 and the Abstract in Okita teach that Input-Side Transformation Circuits 116 receives one of the predetermined number of Reed-Solomon and BCH codes that each have predetermined external Galois-field representations in $GF_b(2^m)$ and translates the external Galois-field representation of the received code into an internal Galois-field representation $GF_a(2^m)$; Note; Figure 2 of Okita teach that if α is the root of the m^{th} order field generation polynomial of $GF_a(2^m)$, then $\beta=\alpha^p$ is the root of the m^{th} order field generation polynomial of $GF_b(2^m)$, hence the Input-Side Transformation Circuits 116 is a translator for translating data from one Galois Field to another); a syndrome

computation module for calculating syndromes comprising intermediate values required to find error locations and values (col. 6, lines 65-67 in Okita teach that Figure 4 is a syndrome generator circuit and col. 2, lines 45-47 in Okita teach that the syndrome generator circuit is used to generate syndromes for use in the Berlekamp-Massey algorithm to find error positions and values), a Berlekamp-Massey computation module that implements a Berlekamp-Massey algorithm that converts the syndromes to intermediate results comprising lambda and omega polynomials (the Berlekamp-Massey algorithm is inherently an algorithm for converting syndromes to intermediate results comprising error locator, lambda, and error magnitude, omega, polynomials); a Chien module comprising modified Chien-search algorithm to calculate actual error locations and error values that correspond to an error-corrected code (Col. 20, lines 46-57, Okita); and an inverse translator circuit for translating the internal Galois-field representation of the error-corrected code into the external Galois-field representation (Output-Side Transformation circuit 120 in Figure 1 of Okita is an inverse translator circuit for translating the internal Galois-field representation of the error-corrected code into the external Galois-field representation).

However Okita does not explicitly teach the specific use of a Chien-Forney module using Forney algorithms to calculate error values.

Cameron, in an analogous art, teaches using Forney algorithms to calculate error values (Forney algorithm circuit 15 in Cameron). One of ordinary skill in the art at the time the invention was made would have been highly motivated to combine the teachings of the Okita patent with the teachings in the Cameron patent since the error

correction system in the Okita patent requires a means for determining error values and Forney's algorithm is a well-known means, that one of ordinary skill would have been apprised of, for determining error values. Note: Cameron explicitly teaches how a modified Berlekamp-Massey algorithm can replace the traditional Berlekamp-Massey algorithm to calculate the error position Lambda polynomial (col. 4 in Cameron). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Forney with the teachings of Cameron by including use of a Chien-Forney module using Forney algorithms to calculate error values. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a Chien-Forney module using Forney algorithms to calculate error values would have provided the opportunity to implement the Error correction system in the Okita patent by including a required means for determining error values.

35 U.S.C. 103(a) rejection of claims 2 and 15.

Figure 1 and the Abstract in Okita teach that Input-Side Transformation Circuits116 receives one of the predetermined number of Reed-Solomon and BCH codes that each have predetermined external Galois-field representations in $GF_b(2^m)$ and translates the external Galois-field representation of the received code into an internal Galois-field representation $GF_a(2^m)$; Note; Figure 2 of Okita teach that if α is the root of the m^{th} order field generation polynomial of $GF_a(2^m)$, then $\beta=\alpha^p$ is the root of the m^{th} order field generation polynomial of $GF_b(2^m)$, hence the Input-Side Transformation Circuits116 is a

translator for translating data from one Galois Field to another. Note also that a quadratic subfield is a particular embodiment for the teachings in the Okita patent since α and β are roots of any m^{th} order field generation polynomial, which includes quadratic polynomials.

35 U.S.C. 103(a) rejection of claims 3, 4, 16 and 17.

Okita and Cameron substantially teaches the claimed invention described in claims 1, 2, 14 and 15 (as rejected above).

However Okita and Cameron do not explicitly teach the specific use of specific circuit elements for carrying out the Berlekamp-Massey Algorithms in the Okita and Cameron patents.

The Examiner asserts that one of ordinary skill in the art at the time the invention was made would have known how to design a circuit for implementing the Berlekamp-Massey Algorithms in the Okita and Cameron patents based on obvious Engineering circuit design choices requirements such as available materials, circuit layout and timing requirements.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Okita and Cameron by including use of specific circuit elements for carrying out the Berlekamp-Massey Algorithms in the Okita and Cameron patents. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of specific circuit elements for carrying out the

Berlekamp-Massey Algorithms in the Okita and Cameron patents would have provided an opportunity for implementing the Berlekamp-Massey Algorithms in the Okita and Cameron patents based on obvious Engineering circuit design choices requirements such as available materials, circuit layout and timing requirements.

35 U.S.C. 103(a) rejection of claim 5.

Col. 2, lines 15-18 in Okita teach that the conventional RS coding/decoding device also has inverse element operation circuits 12a-12x for division operations corresponding to the various codes.

35 U.S.C. 103(a) rejection of claim 6.

Note: there is no indication that the Cameron patent uses any offsets in the code generator polynomial. Cameron teaches an inversionless decoding algorithm (col. 4, lines 47-54, Cameron).

35 U.S.C. 103(a) rejection of claim 8.

See switch 118 in Figure 1 of Okita.

35 U.S.C. 103(a) rejection of claim 10.

Col. 5, 26-37 and Figure 1 in Okita is a Reed-Solomon error correction decoder for decoding a predetermined number of Reed-Solomon codes, hence internal registers in computation circuitry of Figure 1 of Okita is shared among different code types.

35 U.S.C. 103(a) rejection of claims 13 and 19.

Cameron teaches that the degree of the error locator polynomial is tracked (col. 6, lines 15-20, Cameron) and the number of correctable and non-correctable errors is always tracked in any decoding algorithm for BCH and Reed-Solomon codes.

35 U.S.C. 103(a) rejection of claim 11.

Okita and Cameron substantially teach the claimed invention described in claims 1-6, 8 and 10 (as rejected above).

However Okita and Cameron do not explicitly teach the specific use of specific circuit elements for carrying out the Berlekamp-Massey Algorithms in the Okita and Cameron patents.

The Examiner asserts that one of ordinary skill in the art at the time the invention was made would have known how to design a circuit for implementing the Berlekamp-Massey Algorithms in the Okita and Cameron patents based on obvious Engineering circuit design choice requirements such as available materials, circuit layout and timing requirements.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Okita and Cameron by including use of specific circuit elements for carrying out the Berlekamp-Massey Algorithms in the Okita and Cameron patents. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the

art would have recognized that use of specific circuit elements for carrying out the Berlekamp-Massey Algorithms in the Okita and Cameron patents would have provided an opportunity for implementing the Berlekamp-Massey Algorithms in the Okita and Cameron patents based on obvious Engineering circuit design choice requirements such as available materials, circuit layout and timing requirements.

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okita; Shigeru (US 6378104 B1) and Cameron; Clifton J. (US 5905740 A) in view of Vaccaro; John J. et al. (US 5323402 A, hereafter referred to as Vaccaro).

35 U.S.C. 103(a) rejection of claim 7.

Okita and Cameron substantially teaches the claimed invention described in claims 1-6 (as rejected above).

However Okita and Cameron does not explicitly teach the specific use of a systolic decoder (Note: claim 7 is basically directed at capturing elements of a systolic decoder).

Vaccaro, in an analogous art, teaches a systolic decoder (see Abstract, Vaccaro).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Okita and Cameron with the teachings of Vaccaro by including use of a systolic decoder. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a systolic decoder would have provided the opportunity to speed-up error correction.

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okita; Shigeru (US 6378104 B1) and Cameron; Clifton J. (US 5905740 A) in view of White; Philip E. (US 5754563 A).

35 U.S.C. 103(a) rejection of claim 9.

Okita and Cameron substantially teaches the claimed invention described in claims 1-8 (as rejected above).

However Okita and Cameron do not explicitly teach the specific use of dual mode operations.

White, in an analogous art, teaches N channels for parallel processing N blocks of encoded data (Figure 1 in White; Note: if N=2 then the processor in Figure 1 is a dual processor).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Okita and Cameron with the teachings of White by including use of dual mode operations. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of dual mode operations would have provided the opportunity for processing data in parallel.

6. Claims 12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okita; Shigeru (US 6378104 B1) and Cameron; Clifton J. (US 5905740 A) in view of Vaccaro; John J. et al. (US 5323402 A, hereafter referred to as Vaccaro).

35 U.S.C. 103(a) rejection of claims 12 and 18.

Okita and Cameron substantially teaches the claimed invention described in claims 1-11 and 14-17 (as rejected above).

However Okita and Cameron do not explicitly teach the specific use of a systolic decoder (Note: a systolic decoder combined with the transformation circuits in Okita are capable of decoding Reed-Solomon codes using code-generator polynomials having any offset and skip values).

Vaccaro, in an analogous art, teaches a systolic decoder (see Abstract, Vaccaro).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Okita and Cameron with the teachings of Vaccaro by including use of a systolic decoder. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a systolic decoder would have provided the opportunity to speed-up error correction.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Okita; Shigeru (US 6550035 B1) teaches a Reed-Solomon

encoding device is provided that can handle multiple RS (Reed-Solomon) codes using different field generation polynomials.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Art Unit 2133